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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
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| 09/410,202 | 09/30/99 | DONOVAN | B 7134.007 |

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| ART UNIT | PAPER NUMBER |
| 2155 | 4 |

TM02/1102
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DATE MAILED: 11/02/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

T.K

| Office Action Summary | Application No. 09/410,202 | Applicant(s) DONOVAN, BRIAN | |
|---|---|---|---|
| | Examiner DAVID Y. ENG | Art Unit 2155 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8/25/2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *1 and 3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-9* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claim1, drawn to a method for switching between tasks, classified in class 709, subclass 100.

II. Claims 2 and 4-9, drawn to a emthod and apparatus for ordering tasks for execution, classified in class 709, subclass 103.

III. Claim 3, drawn to a computer for storing record of executed instructions, classified in class 714, subclass 45.

Inventions I , II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as in a computer system which does not require task ordering in a manner as recited in claim 2 and inventions I and II each has separate utility such as in a computer system which does not require recording as recited in claim 3. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with William Geny on October 30, 2001 a provisional election was made without traverse to prosecute the invention of Group II, claims 2 and 4-9. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1

and 3 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claims 2, 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the incrementing step is not clear. It appears that the relative priority levels between tasks are not changed if each priority level is incremented as a function of time.

In claim 7, it is not seen how the timer as recited in claim 7 is related to determining readiness for execution as recited in parent claim 4.

In claim 8, it is not seen how tracing as recited in claim 8 is related to task switching recited in parent claim 4. Further, there is no antecedent basis for "register states" in claim 8.

Claim 9 has similar defects. It appears that the multiplexing circuit, the first set of latches and the task switch controller as recited therein are unrelated to task switching.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madnick (text book Operating System, McGraw-Hill, 1974).

See pages 209-240 in Madnick.

With respect to claims 2 and 4, Madnick discloses a method and apparatus for ordering the performance of tasks in a computer system, comprising:

A job schedular and a process schedular (4-1.1) (4-1.2) (4-2.2)(4-2.5)(4-3)(4-3.1) (4-3.2),

a. for maintaining a priority level for each task or for determining whether a task is ready for execution,

b. for determining an order for the running of tasks (4-2)(4-2.3.1)(4-2.3.2), and

c. for controlling the execution of tasks in a sequence inaccordance with the priority.

With respect to claims 2 and 5, Madnick did not explicitly teach that priority level can be incremented as a function of time. However, Madnick does teach, in line 7 of section 4-3.2 (page 237), that inter alia, slapsing of a time quantum can be a factor for determining priority policy. From the teaching, one of ordinary skill in the art would readily recognize that priority level of a task can be incremented as a function of time.

With respect to claim 6, task linking is an inherent circuit of a task scheduler because all tasks are to be executed in a priority sequence determined by the scheduler.

With respect to claim 7, see sections 4-1.2 on pages 212 and 213, Madnick teaches task interrupts for storing register state in multiprocessing (see policy 2 and 3).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madnick in view of George (4,888,691).

Madnick teaches claim limitations set forth above. Madnick does not have a trace for redording state informations. However, George teaches a trace circuit for recording state information when interrupts happened. See column 3 et seq lines 19 and column 21 et seq lines 25. Since both references are directed toward interrupt, it would have been obvious to a person of ordinary skill in the art to incorporate a trace circuit in Madnick such that state information can be retrieved later for analysis.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madnick in view of Jen (3,789,365).

Madnick teaches claim limitations set forth above. Madnick does not have multiplexer for storing and switching. See Figure 1 in Jen. Jen discloses an interrupt system having multiplexers (18A, 19A and 16A etc.) for storing and and switching tasks. Since both references are directed toward interrupt, it would have been obvious to a person of ordinary skill in the art to incorporate a multiplexer as taught by Jen in Madnick such that interrupt latency can be improved.

DAVID Y. ENG
PRIMARY EXAMINER